High Mobility Flexible Graphene Field-Effect Transistors with Self-Healing Gate Dielectrics

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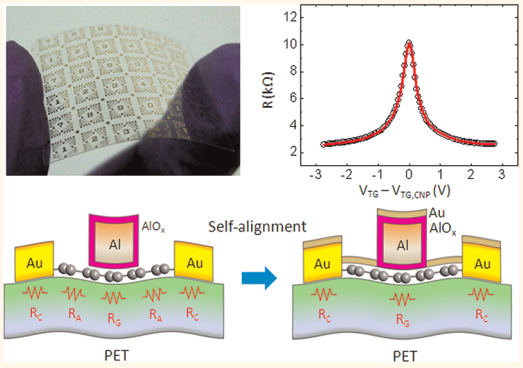
ABSTRACT



A high-mobility low-voltage graphene field-effect transistor (FET) array was fabricated on a flexible plastic substrate using high-capacitance natural aluminum oxide as a gate dielectric in a self-aligned device configuration. The high capacitance of the native aluminum oxide and the self-alignment, which minimizes access resistance, yield a high current on/off ratio and an operation voltage below 3 V, along with high electron and hole mobility of 230 and 300 $cm^2/V \cdot s$, respectively. Moreover, the native aluminum oxide is resistant to mechanical bending and exhibits self-healing upon electrical breakdown. These results indicate that self-aligned graphene FETs can provide remarkably improved device performance and stability for a range of applications in flexible electronics.

KEYWORDS: graphene · field-effect transistor · self-alignment · chemical vapor deposition · flexible electronics

One of the obstacles to the development of flexible electronics has been creating transistors with high carrier mobility, yet stable enough to function in a variety of environments. Organic semiconductor materials offer a flexible platform for use as active components in field-effect transistors (FETs), opening up a variety of promising applications in lightweight, low-cost, and low-power switching components, such as active-matrix elements for plastic displays,[1−4] sensor arrays,[5,6] radio frequency identification tags,[7] and flexible logic circuits.[8,9] However, the carrier mobility of organic materials is low, typically ranging from 10^{-3} to 1 $cm^2/V \cdot s$ due to the weak van der Waals interaction between π-conjugated molecules leading to hopping conduction. Graphene is a single-atomic layer macromolecule with promise as a high-speed platform for flexible and transparent FETs built on soft substrates. Chen *et al.* reported fabricating flexible graphene FETs *via* the transfer printing method, transferring mechanically exfoliated graphene flakes and predefined electrodes to a plastic substrate for device assembly.[10] For practical applications, large-scale graphene films grown by chemical vapor deposition (CVD) are desirable, as is fabrication compatibility with silicon technology. Currently, flexible FETs using CVD graphene as a channel material have only exhibited an electron mobility of ~90 $cm^2/V \cdot s$.[11] This is presumably due to the long access lengths (*i.e.*, the ungated channel region between the drain/source contacts and gate), downgrading device performance through the parasitic resistance R_A.[12] Farmer *et al.* showed that self-aligned top gates fabricated using the hydrophobic characteristics of the surface of exfoliated graphene can minimize the access length,[12] yielding a greatly increased carrier mobility and cutoff frequency in the resulting FETs. However, the hydrophobic surface of large-area CVD graphene is usually obscured by a thin layer of polymer residue due to the transfer process.[13,14] The inhomogeneous coverage of the polymer residue frequently results in pinholes in the stack of high-κ dielectrics (*e.g.*, Al_2O_3, HfO_2, and ZrO_2) grown by atomic layer deposition (ALD). The high temperatures used in the ALD process may also rule out the use of some plastic substrates.[15−17]

This paper describes the fabrication of self-aligned CVD graphene FETs on a plastic substrate, using naturally formed aluminum oxide as a gate dielectric and spacer for self-alignment. The fabrication process is not

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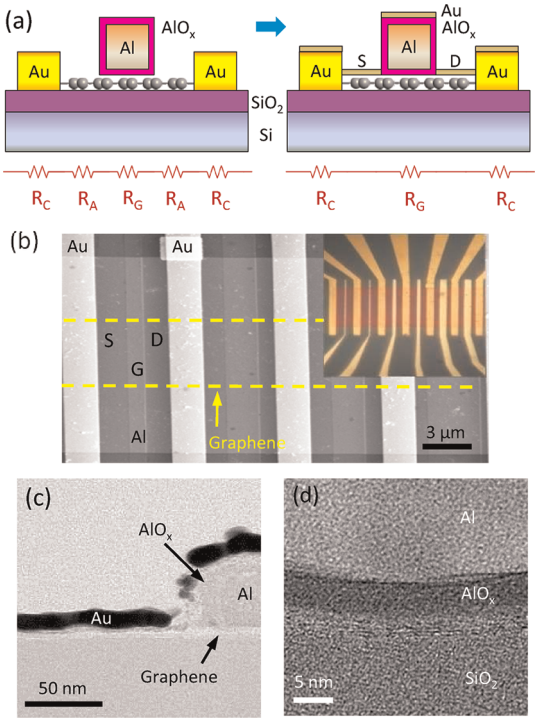

Figure 1. (a) Schematic diagram of the steps used to fabricate self-aligned graphene FETs on a Si substrate. The lower panel shows the critical resistive components before and after the self-alignment. (b) SEM image of self-aligned graphene FETs with different gate lengths (300 nm, 700 nm, and 2 μm). The channel width of all devices is 10 μm. The optical photograph in the inset shows the overall device layout. The self-aligned source/drain electrodes are separated by AlO$_x$ spacers in each device. (c) TEM image of the detailed device layout in the vicinity of AlO$_x$ spacer. (d) TEM image of AlO$_x$ grown deeply at the interface between graphene and Al.

restricted by graphene surface characteristics, and hence neither predefined buffer layers nor chemical functionalization on the graphene surface are required prior to the deposition of gate dielectrics. The access resistance in the graphene channels is minimized, resulting in high electron mobility that is potentially comparable with exfoliated graphene on SiO$_2$/Si, and does not degrade upon bending to a radius $R > 8$ mm. The natural AlO$_x$ possesses high gate capacitance and exhibits the unique property of self-healing upon electrical breakdown. The damaged alumina dielectric layer can be healed using mild electrical annealing or aging in air, both repairing the dielectric without noticeable increase in leakage current or downgrading of electron mobility.

RESULTS AND DISCUSSION

Before fabricating graphene FETs on plastic substrate, we first produced graphene FETs on Si substrate with dual gates to better characterize the alumina gate dielectric. The cross-sectional device layout is schematically shown in the left panel of Figure 1a. In the conventional top-gated graphene FETs, a long access length usually exists between the gate and drain/source electrodes. The ungated graphene channel stays in a highly resistive state because the Fermi level is located in the vicinity of the conical points of band structure, which possess low density of electronic states. It results in a total resistance which consists of contact resistance R_C, access resistance R_A, and gated resistance R_G, as schematically shown in the lower left panel of Figure 1a. The access resistance usually turns out to be a dominant component in the total resistance as downscaling the graphene FET and negatively impacts device performance. It is therefore desirable to shorten the access length as much as possible. For a graphene FET with dual gates, a facile way to modulate the carrier density in the access graphene channel is by applying a back-gate voltage. However, it becomes inaccessible for graphene FETs built on a nonconductive plastic substrate. To minimize R_A in a single-gating configuration, fabrication of self-aligned drain/source contacts provides a technically feasible solution and can be applied to all sources of planar graphene and plastic substrates.

Graphene used for device fabrication was grown by low-pressure CVD technique on Cu foil,[18] followed by a wet transfer process using poly(methyl methacrylate) (PMMA) as a scaffold. Detailed graphene characterizations can be found in Supporting Information. A graphene strip was then defined by e-beam lithography in combination with oxygen plasma etching. Source/drain electrodes (0.5 nm Cr/60 nm Au) and an Al top gate (70 nm) were made by two-step e-beam lithography and thermal evaporation. No additional dielectric layer between the Al and graphene was introduced. Following Al evaporation, the devices were exposed to air for at least 6 h to form a thin AlO$_x$ dielectric layer around the Al wire.[19,20] Another layer of Cr (0.5 nm)/Au (10 nm) was deposited on a patterned region, completely covering the graphene strip. This deposition was automatically aligned by the Al/AlO$_x$ gate edges and separated into two isolated regions, forming the source and drain electrodes. This process reduced the access length to ~20 nm, mainly the length underneath the spacer.

Figure 1b shows a scanning electron microscopy (SEM) image of self-aligned graphene FETs on a Si substrate with different gate lengths, while the inset shows an optical photograph of the overall device layout. For the self-alignment, the spacers that separate source/drain from gate electrode are constituted of natural AlO$_x$, which is electrically robust and exhibits the unique feature of self-healing upon breaking down. Figure 1c shows the cross-sectional transmission electron microscopy (TEM) image of a spacer. The source/drain electrodes are well separated by the Al/AlO$_x$ gate electrode and are precisely positioned next to the spacers. The average access length measured by TEM is about 20 nm. Figure 1d shows a high-resolution TEM image of the AlO$_x$/graphene interface. The AlO$_x$

layer is found to form around the Al wire and penetrates deep into the interface between the Al and graphene following exposure to air over 6 h at room temperature. The oxidation can be expedited using current-induced annealing. The thickness of the oxide layer ranges from 5 nm (embedded at the graphene/Al interface) to 12 nm (exposed to the air) (see Supporting Information for more details). The natural AlO_x on CVD graphene provides a negligible leakage current within the gate sweep range of ±2.5 V, while typical leakage current is <100 pA. Compared with organic FETs using natural AlO_x as a gate dielectric, the leakage current in our CVD graphene FETs is noticeably suppressed. This is attributed to the presence of residual PMMA (1−2 nm) on the graphene,[13,14] which resembles the self-assembled monolayer on AlO_x as a hybrid dielectric.[5,21,22]

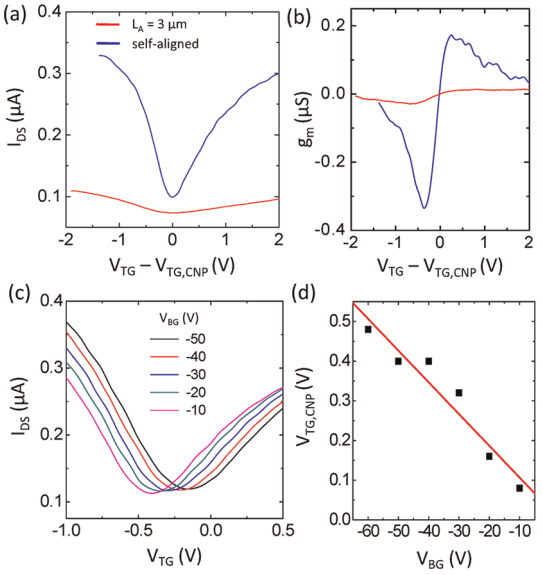

Figure 2. Device properties of self-aligned graphene FETs on a silicon substrate. (a) Transfer characteristics of a device before (red curve) and after (blue curve) self-alignment. (b) Corresponding transconductance of the curves shown in (a). (c) Transfer characteristics of a self-aligned device. The bottom-gate is swept between −10 and −50 V in 10 V steps. (d) Dirac voltage varies linearly with the top- and back-gate voltages.

Figure 2a,b shows the impact of self-alignment on the same CVD graphene transistor with a channel width $W = 5\ \mu m$ and channel length $L = 2\ \mu m$. A total access length of 4 μm is eliminated following self-alignment. The transfer characteristics and corresponding transconductances of the device show the benefits of self-alignment. Following self-alignment, the maximum I_{ON}/I_{OFF} ratio is increased from 1.2 to 3.2, and the maximum transconductance, $g_m = |dI_{DS}/dV_G|$, also rises by an order of magnitude at $V_{DS} = 1$ mV for both electron and hole. To better understand device performance, the top-gate dielectric capacitance C_{TG} is obtained by measuring the drain current at varying top-gate V_{TG} or back-gate V_{BG} sweeps (Figure 2c). The charge neutrality point at each V_{TG} sweep ($V_{TG,CNP}$) exhibits a linear shift as a function of the V_{BG} (Figure 2d), from which we can determine C_{TG} using the simple capacitance equation, $Q = CV$. The top-gate capacitance is written as $C_{TG} = -C_{BG}(\Delta V_{BG}/\Delta V_{TG})$, yielding $C_{TG}/C_{BG} \approx 86$ from the slope of Figure 2d. For 300 nm thick SiO_2, C_{BG} is 11.6 nF/cm^2. The top-gate dielectric capacitance is found to be $C_{TG} = 998$ nF/cm^2. Using the capacitance model for parallel plates, the permittivity of the AlO_x layer is determined to be $\varepsilon_{TG} = C_{TG}d_{TG}/\varepsilon_0 = 5.65$ for $d_{TG} = 5$ nm, a value typically found in a natural AlO_x thin film.[23]

Figure 3a shows the flexibility of self-aligned graphene FETs fabricated on poly(ethylene terephthalate) (PET),

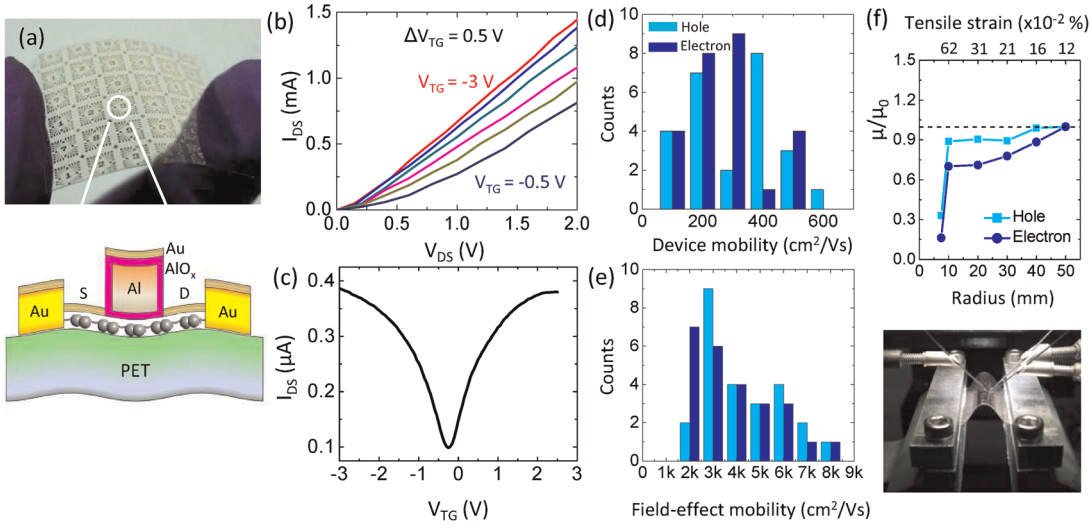

Figure 3. Electrical and mechanical properties of self-aligned graphene FETs fabricated on a flexible substrate. (a) Optical photograph of an array of devices on a PET substrate, with a schematic drawing showing the device layout. (b) Output characteristics of graphene FETs on PET. The gate voltage was applied between −0.5 and −3 V in −0.5 V increments. (c) Transfer characteristics of graphene FETs on PET. (d) Histogram of device mobility. (e) Histogram of intrinsic field-effect mobility. (f) Normalized mobility as a function of the bending radius and tensile strain.

using the same fabrication process as that used for devices made on rigid substrates (details are provided in the Supporting Information). Figure 3b,c shows the typical output and transfer characteristics of the resulting devices. No apparent degradation of device characteristics is found as compared with those fabricated on SiO_2. This is attributed to the fact that graphene devices fabricated on SiO_2 suffer from additional scattering associated with low-energy surface phonon. Substantial trap density in SiO_2 also results in appreciable decrease of device mobility. However, for the graphene lying on the PET substrate, the nanoscale surface roughness (see Supporting Information) makes the transferred graphene film semisuspended, mitigating the surface phonon and trapped charge scatterings. Although the carrier mobility may be deteriorated by the local strains, the measured intrinsic carrier mobility on PET is found to be similar to that on SiO_2. The charge neutrality point in the transfer characteristics deviates from $V_{TG} = 0$ due to the weak electron doping of the gate.[24,25] The I_{ON}/I_{OFF} ratio falls in the range of 3−6, and the g_m is 300−500 nS. Using $\mu_{DEV} = g_m L/V_{DS} W C_{TG}$, these transconductances can be translated into device mobilities, as shown in Figure 3d. The respective mean device mobilities for electron and hole are 230 and 300 $cm^2/V \cdot s$. Compared with other reported flexible FETs, such as amorphous silicon, polycrystalline silicon, organic materials, and carbon nanotubes, our self-aligned flexible graphene FETs exhibit improved mobility (see Supporting Information). To gain further insight into the intrinsic carrier mobility, we adopt the model described in ref 26 to fit the transfer characteristics in the form of a $R_{DS}-V_{TG}$ plot. The device's total resistance R_T can be expressed using the following equation which contains the contact resistance R_C, access resistance R_A, and the intrinsic graphene channel resistance covered by the gate electrode:

$$R_T = 2R_C + 2R_A + \frac{L_G}{We\mu_{FE}\sqrt{n_0^2 + n_{TG}^2}}$$

where L_G and n_0, respectively, are the gate length and residual carrier density at the charge neutrality voltage. The carrier density induced by the top gate is calculated with $n_{TG} = C_{TG}(V_{TG} - V_{TG,CNP})/e$. Figure 3e shows the histogram of field-effect mobility refitted using the above equation. Each fitting gives the residual carrier density n_0, $2(R_C + R_A)$, and field-effect mobility μ_{FE}. Due to the negligible R_A in the self-aligned devices, their series resistance is dominated by the metal contacts. The mean contact resistance R_C in our devices is ~2 kΩ. The μ_{FE} increases by an order of magnitude after subtracting the contact resistance and ranges from 2000 to 8000 $cm^2/V \cdot s$. The wide mobility distribution may result partly from the variation of graphene quality such as the formation of bi- and trilayer graphene in part of the large-area graphene film (Figure S2 in Supporting Information) and partly from the inhomogeneous PMMA residue that causes substantial variation of the hybrid gate capacitance. The high contact resistance is responsible to the low device mobility shown in Figure 3d. Lowering the contact resistance is, therefore, as important as minimizing the access resistance so as to obtain high device mobility in graphene FETs. It was also found that bending the substrate to a radius of $R > 8$ mm does not cause apparent changes in the $R_{DS}-V_{TG}$ curves or the mobility (Figure 3f), indicating that bending causes no degradation in the graphene channel or contacts.

The natural AlO_x not only acts as the spacer for self-alignment but also self-heals upon electrical breakdown.[27] To explore the self-healing of alumina on graphene, dielectric breakdown was intentionally triggered by progressively increasing the gate−source voltage to exceed the breakdown field. The dielectric strength of a material is essentially dependent on the configuration of the material or the electrodes by which the field is applied. For natural alumina formed on transferred CVD graphene, the breakdown field is ~5 MV/cm, provided that the breakdown occurs at the thinnest part. Dielectric breakdown results in an abrupt and considerable increase of current flowing through the oxide (Figure 4a,b), and the V-shaped ambipolar conduction vanishes in the gate sweeps due to the loss of potential modulation by the gate. At the high field, the $I-V_{GS}$ curves become irreversible, indicating physical damage such as pinholes or nanocracks in the oxide.

The damaged oxide can be restored automatically through several hours of air exposure or alternatively through electrical annealing to expedite the healing rate (see Supporting Information). Fresh native oxide can regenerate in the vicinity of the damaged areas, though the gate oxide is sandwiched by graphene and aluminum, effectively reducing the leakage current to a level comparable to that of the pristine state. The lower panels in Figures 4a and 4c compare the transfer characteristics of a device before and after self-healing in air, showing that device properties including current on/off ratio, transconductance, and charge mobility are nearly fully restored following the repair. For self-healing by aging in air, temperature and humidity are the major parameters that affect the reaction rate. Generally, it takes ~6 h to regrow the native oxide to sufficient thickness, indicating that diffusion of H_2O or O_2 into the graphene/Al interface is the rate-limiting step. It should be noted that the involvement of H in the oxide creates electronic defects[28] that tail a few electronvolts from the band edges to deep within the oxide gap.[29] At the high field, electronic conduction (gate leakage) can occur *via* carrier tunneling through the triangular barrier into a defect level in the oxide.[30] It is, therefore, possible to assess the quality of the

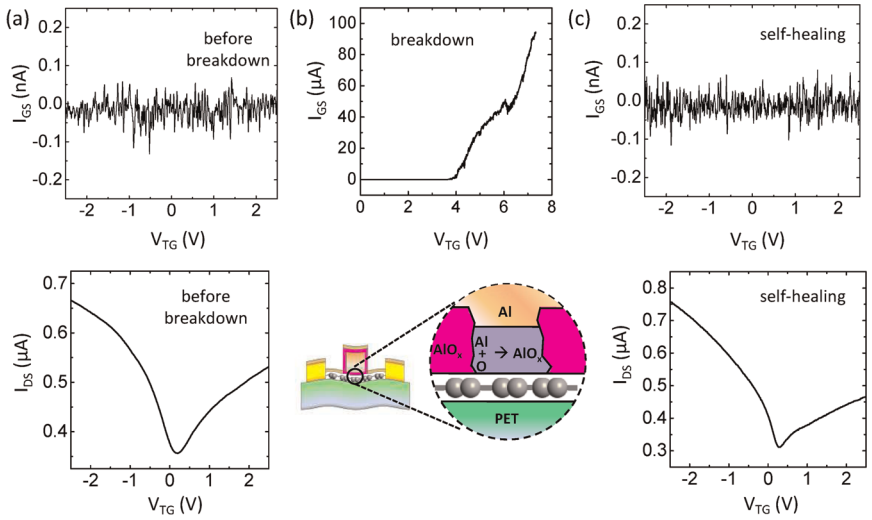

Figure 4. $I_{GS}-V_{GS}$ and $I_{DS}-V_{GS}$ curves of a graphene FET on PET. (a) Before the AlO_x dielectric breakdown. (b) $I_{GS}-V_{GS}$ curve at the breakdown. The lower panel is a schematic drawing showing the regrowth of native AlO_x at the breakdown site. (c) Following self-healing of the AlO_x layer by aging in air for 6 h.

natural aluminum oxides from the $I_{GS}-V_{TG}$ curve shown in Figure 4b.

CONCLUSIONS

We present a type of flexible graphene FET with a self-aligned gate. The naturally formed aluminum oxide acts as a high-quality gate dielectric and spacer for the formation of self-aligned drain/source contacts. This self-aligned process can be applied to different graphene sources, irrespective of graphene surface conditions, thus allowing for device fabrication using large-area CVD graphene, even with polymer residues on the surface. The access length is greatly reduced to 20 nm, resulting in relatively high device mobilities of 150−230 and 260−300 $cm^2/V\cdot s$, respectively, for electron and hole. Moreover, the aluminum gate provides low-voltage device operation, which should facilitate future implementation of logic gates. This method represents a significant step in the application of graphene to flexible electronics.

METHODS

Graphene Growth. Graphene sheets used in the current study were grown by low-pressure CVD of methane (99.99%) on polycrystalline Cu foils. Prior to growth, the Cu foils were cleaned by acetone and isopropyl alcohol (IPA) with sonication, followed by etching in acetic acid for 30 min to remove surface oxides. Then, the Cu foil was mounted in the CVD chamber with a steady flow of 10 sccm hydrogen. The furnace was ramped up to 1000 °C over 40 min. In the CVD process, methane (20 sccm) mixed with hydrogen (10 sccm) was fed into the reaction chamber for 10 min at the pressure of about 2.1 Torr. After the growth, the Cu foil was moved to the cooling zone without changing the hydrogen flow. The characterization results of our CVD graphene are provided in Supporting Information.

Device Fabrication. Graphene FETs were made with e-beam lithography and standard lift-off process. PMMA in a two-layer structure (996 and 120 K) was spin-coated on the graphene film, followed by baking at 130 °C for 30 min. E-beam lithography was carried out using a scanning electron microscope (JSM-840A) equipped with an e-beam writer (Elphy Quantum, Raith). The exposed PMMA was then developed with methyl isobutyl ketone (MIBK) and IPA in a ratio of 1:3. Metal contacts were evaporated after the development. Keithley 2400 and 2000 were, respectively, used as a current/voltage source and multimeter for current−voltage measurements. All of the devices were measured in ambient conditions in a two-probe configuration.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Additional graphene characterizations, process flow of device fabrication, and electron tunneling through the Al/AlO_x/graphene junction are given in Figures S1−S8. Mobility comparison with other reported flexible FETs is given in Table S1. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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